

## CLAIMS

What is claimed is:

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1. A method for processing an instruction within a processor, the method comprising:

executing an instruction within the processor; and  
in response to completion of the executed

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instruction, automatically writing by the processor a copy of the executed instruction or an opcode of the executed instruction to a register within the processor.

2. The method of claim 1 wherein the register is a dedicated-purpose register that is used to hold executed instructions.

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3. The method of claim 1 further comprising:

determining whether or not an enable flag was

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previously set prior to writing the executed instruction or its opcode to a register within the processor.

4. The method of claim 1 further comprising:

determining whether or not an interrupt-enable flag

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is set prior to writing the executed instruction or its opcode to a register within the processor.

5. The method of claim 1 wherein the register is one of a plurality of registers that are used to hold executed instructions or their opcodes.

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6. The method of claim 1 further comprising:  
determining whether or not a taken-branch flag is  
set prior to writing the executed instruction or its  
opcode to a register within the processor.

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7. The method of claim 1 further comprising:  
reading the register by tracing software to obtain a  
copy of the executed instruction or its opcode; and  
writing the copy of the executed instruction or its  
opcode to persistent storage.

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8. A method for processing an instruction within a processor, the method comprising:

executing an instruction within the processor; and  
in response to completion of the executed  
5 instruction, automatically writing by the processor a  
copy of the executed instruction or an opcode of the  
executed instruction to a memory buffer.

9. The method of claim 8 further comprising:

10 reading a register within the processor to obtain a  
pointer to the memory buffer.

10. The method of claim 8 further comprising:

15 writing a memory address for the memory buffer to a  
register within the processor.

11. The method of claim 8 further comprising:

20 determining whether or not a taken-branch flag is  
set prior to writing the executed instruction or its  
opcode to the buffer in memory.

12. The method of claim 8 further comprising:

25 reading the memory buffer by tracing software to  
obtain copies of executed instructions or their opcodes;  
and

writing the copies of executed instructions or their  
opcodes to persistent storage.

13. A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

5 means for fetching instructions from memory;

means for executing an instruction within the processor; and

means for automatically writing by the processor a copy of the executed instruction or an opcode of the executed instruction to a register within the processor in response to completion of the executed instruction.

14. The processor of claim 13 wherein the register is a dedicated-purpose register that is used to hold executed instructions.

15. The processor of claim 13 further comprising:

means for determining whether or not an enable flag was previously set prior to writing the executed instruction or its opcode to a register within the processor.

16. The processor of claim 13 further comprising:

means for determining whether or not an interrupt-enable flag is set prior to writing the executed instruction or its opcode to a register within the processor.

17. The processor of claim 13 wherein the register is one of a plurality of registers that are used to hold executed instructions or their opcodes.

18. The processor of claim 13 further comprising:

means for determining whether or not a taken-branch  
flag is set prior to writing the executed instruction or  
5 its opcode to a register within the processor.

19. The processor of claim 13 further comprising:

means for reading the register by tracing software  
to obtain a copy of the executed instruction or its  
10 opcode; and

means for writing the copy of the executed  
instruction or its opcode to persistent storage.

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20. A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

means for fetching instructions from memory;

5 means for executing an instruction within the processor; and

means for automatically writing by the processor a copy of the executed instruction or an opcode of the executed instruction to a memory buffer in response to completion of the executed instruction.

21. The processor of claim 20 further comprising:

means for reading a register within the processor to obtain a pointer to the memory buffer.

22. The processor of claim 20 further comprising:

means for writing a memory address for the memory buffer to a register within the processor.

23. The processor of claim 20 further comprising:

means for determining whether or not a taken-branch flag is set prior to writing the executed instruction or its opcode to the buffer in memory.

24. The processor of claim 20 further comprising:

means for reading the memory buffer by tracing software to obtain copies of executed instructions or their opcodes; and

means for writing the copies of executed instructions or their opcodes to persistent storage.

25. A computer program product in a computer-readable medium for use in a processor, the computer program product comprising:

means for executing an instruction within the processor; and

means for automatically writing by the processor a copy of the executed instruction or an opcode of the executed instruction to a register within the processor in response to completion of the executed instruction.

26. The computer program product of claim 25 wherein the register is a dedicated-purpose register that is used to hold executed instructions.

27. The computer program product of claim 25 further comprising:

means for determining whether or not an enable flag was previously set prior to writing the executed instruction or its opcode to a register within the processor.

28. The computer program product of claim 25 further comprising:

means for determining whether or not an interrupt-enable flag is set prior to writing the executed instruction or its opcode to a register within the processor.

29. The computer program product of claim 25 wherein the register is one of a plurality of registers that are used to hold executed instructions or their opcodes.

30. The computer program product of claim 25 further comprising:

5 means for determining whether or not a taken-branch flag is set prior to writing the executed instruction or its opcode to a register within the processor.

31. The computer program product of claim 25 further comprising:

10 means for reading the register by tracing software to obtain a copy of the executed instruction or its opcode; and

means for writing the copy of the executed instruction or its opcode to persistent storage.

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32. A computer program product in a computer-readable medium for use in a processor, the computer program product comprising:

means for executing an instruction within the processor; and

means for automatically writing by the processor a copy of the executed instruction or an opcode of the executed instruction to a memory buffer in response to completion of the executed instruction.

33. The computer program product of claim 32 further comprising:

means for reading a register within the processor to obtain a pointer to the memory buffer.

34. The computer program product of claim 32 further comprising:

means for writing a memory address for the memory buffer to a register within the processor.

35. The computer program product of claim 32 further comprising:

means for determining whether or not a taken-branch flag is set prior to writing the executed instruction or its opcode to the buffer in memory.

36. The computer program product of claim 32 further comprising:

means for reading the memory buffer by tracing software to obtain copies of executed instructions or their opcodes; and

means for writing the copies of executed instructions or their opcodes to persistent storage.

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